UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,300	06/30/2000	Bret S. Weber	98-063	9608

24319 7590 09/24/2002

LSI Logic Corporation
1551 McCarthy Blvd.
M/S: D-106 Patent Department
Milpitas, CA 95035

EXAMINER
TAKEGUCHI, KATHY K

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 09/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,300	WEBER ET AL.	
	Examiner	Art Unit	
	Kathy Takeguchi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The present Office Action is a Non-Final Action taken in response to examination of Claims 1-23, presented in the application. Applicant is reminded that each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in 37 CFR 1.56.

Objections

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors.

The following objection is noted:

In the specification (Background of the Invention, page 1, line 24), "disk drive does render the entire subsystem unusable" should be changed to "disk drive does not render the entire subsystem unusable" or "disk drive does render the entire subsystem usable".

In the specification (Background of the Invention, page 1, line 29), the word—array-- has a single quotation followed by a double quotation.

In the specification (Background of the Invention, page 2, line 7), "RIAD" should be changed to "RAID".

In the specification (Detailed Description of the Preferred Embodiments, page 6, line 22), "a number disk drives" should be changed to "a number of disk drives".

Appropriate correction is required.

Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification, the drawings or the claims.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by Walton et al (United States Patent No. 6389494 B1).

With respect to Claim 1, Walton et al disclose a data storage system for transferring data between a host computer and a bank of disk drives. The storage system contains a front-end controller (director), a back-end controller (director), and an interconnect element coupled to said front-end controller and said back-end controller (e.g., Figure 2; Column 2, line 51 to Column 3, line 6; Column 3, lines 38-48; Column 4 lines 38-42).

Regarding Claim 2, Walton et al further disclose a plurality of disk drives coupled to I/O devices to said back-end controller. Walton's design has rear-end directors, which are connected to a plurality of disk drives, i.e. disk drive bank labeled as 116 (e.g., Figure 2; Column 3, lines 61-63; Column 4, lines 6-14).

With respect to Claim 3, Walton et al suggest a first subset of said plurality of disk drives, a second subset of plurality of disk drives, and a back-end controller composed of a plurality of back-end controllers. Furthermore, Walton et al suggest the coupling of the first pair of back-end controllers to the first subset of disk drives and the coupling of the second pair of back-end controllers to the second subset of disk drives (e.g., Figure 2; Column 3, line 59 to Column 4, line 14). Walton's storage system suggests multiple rear-end directors (e.g., Figure 2; Column 3, line 60-63) in connection with two subsets of memory devices in connection with the disk drive bank (e.g., Figure 2; Column 4, lines 27-34).

With respect to Claim 4, Walton et al suggest a redundant link coupling the first pair of back-end controllers to a first subset and another redundant link coupling said second pair of back-end controllers to said second subset (e.g., in Figure 2, each controller has a connection to each memory subset through Bus 126 in addition to a redundant coupling through either Bus A, Bus B, Bus C, or Bus D to each memory subset).

With respect to Claim 5, Walton et al disclose a front-end control element comprised of a plurality of front-end controllers (e.g., Figure 2), wherein each of said plurality of front-end controllers is coupled to each of said pair of interconnect elements,

which are comprised of a pair of interconnect elements (e.g., Figure 2, Column 3, line 57 to Column 4, line 6).

With respect to Claim 6, Walton et al disclose a first set of disk drives, a second set of disk drives, and a back-end control element comprising a plurality of back-end controllers (e.g., Figure 2; Column 4, lines 6-14). Walton et al suggest a first pair of back end controllers coupled to the first set of disk drives and also to a corresponding one of said pair of interconnect elements. Additionally, Walton et al suggest a second pair of back-end controllers coupled to a corresponding one of said pair of interconnect elements (e.g., Figure 2, Column 3, line 57 to Column 4, line 6).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton et al in view of Computer Architecture: A Quantitative Approach, by Hennessy and Patterson.

With respect to Claim 7, Walton et al teach the system of Claim 1, but do not specifically mention that the bus is a PCI bus. However, the PCI bus is often used for fast I/O devices (Hennessy and Patterson, page 573) as in the system described within the claims. Additionally, it is known in the art that the use of PCI buses is prevalent in I/O

architectures. Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to specify a PCI bus as the interconnect because Hennessy and Patterson claim that within the hierarchy of buses, a PCI bus would provide for a fast interconnect.

With respect to Claim 11, Walton et al disclose a system as described in Claim 1, but do not specify that the (front-end and back-end) control elements and the interconnect elements may be added independently of all other elements. However, due to the redundancy and the parallel connections, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to specify that the control elements (front-end and back-end) along with the interconnect elements may be added independent of all other such elements without hindrance or disruption to the overall, basic system.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton et al in view of Belsan (United States Patent No. 5394532).

With respect to Claim 12, Walton et al teach the system of Claim 1, but do not specifically mention that the front-end control is operable to perform the mapping of logical store addresses to physical store addresses for further operations by said back-end control element. Belsan, however, teaches a control unit connected to both hosts and I/O devices. Belsan's control unit labeled as 101 in Figure 2 is operable to perform the major data storage control functions, which includes the mapping of logical storage addresses to physical storage addresses (e.g., Column 5, lines 8-16; Column 7, lines 36-53; Column 8, lines 47-52). Thus, it would have been obvious at the time the invention was made to a

person having ordinary skill in the art to have a control unit with the ability to map logical storage addresses to physical storage addresses because logical addresses need to be translated or mapped to physical addresses because logical addresses do not relate directly to a physical location. Instead, a controller usually performs a logical to physical address conversion to access the data from the physical location.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Walton et al in view of Computer Architecture: A Quantitative Approach, by Hennessy and Patterson.

With respect to Claim 13, Walton et al teach the system of Claim 1, but do not specifically mention that the back-end control element has a RAID parity assist element for RAID parity generation and checking. Furthermore, Hennessy and Patterson teach the use of parity as a level and an approach to the concept of redundancy for a RAID system (Computer Architecture: A Quantitative Approach, page 521-525). Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to include and specify a back-end control element having a RAID parity assist element because such an element would provide feedback as to the accuracy of the data and for error checking, especially in the transmission of data.

9. Claims 8-10 and Claims 14-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Walton et al in view of Brown et al (United States Patent No. 6148414).

With respect to Claims 8, Walton et al teach the system of Claim 1, but do not specifically mention that the interconnect element comprises a Fibre Channel SAN switch coupled to a Fibre Channel communication medium. Brown et al, however, teach the use of an interconnect element comprising preferably of a Fibre Channel switch coupled to a Fibre Channel communication medium (e.g., Figure 2; Column 6, lines 20-66). Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to combine the teachings of Walton et al and Brown et al to provide for fast, reliable communication channels for transmitting large quantities of data between the host computers and the I/O devices.

With respect to Claims 9 and 10, Walton et al teach the system of Claim 1, but do not specifically mention the use of either an InfiniBand compliant communication medium or a local area network communication medium for an interconnect. Brown et al suggest that a Fibre Channel communication medium is preferable, but also suggest the use of PCI buses and imply the use of other communication mediums (e.g., Column 6, lines 31– 43). Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use an InfiniBand compliant communication medium because InfiniBand provides higher bandwidth and lower latency as compared to a PCI bus. It would also have been obvious at the time the invention was made to a person having ordinary skill in the art to use a local area network communication medium because a local area network communication medium is a basic interconnect medium used for the exchange of information.

With respect to Claim 14, Walton et al teach a front-end control element for a storage subsystem having a processor (e.g., CPU in Figure 4) coupled to a host system

interface (e.g., interface labeled as 118 in Figure 2). Although Walton et al do not specify a SAN interface coupled to said processor for coupling the front-end control element to the back-end control element, Walton et al show the inclusion of a bus interface (e.g., Figure 4), which is coupled to the CPU and to Bus D, providing for the exchange of information between the front-end control element and the back-end control element (e.g., Figure 2). However, Brown et al discuss the use of SAN for the convenience of communication among all the controllers (e.g., Figure 4; Column 7, lines 29-53). Thus, it would have been obvious at the time the invention was made to a person having ordinary skill in the art with the teachings of Walton et al and Brown et al before him to have a front-end control element having a processor coupled to both the host system interface and a SAN interface because the processor could easily transfer data to both interfaces (host and SAN) directly.

With respect to Claim 19, Walton et al discuss a back-end control element for a storage subsystem with the back-end control element coupled to a plurality of disk drives (e.g., Figure 5). Also, there is a system interface between the back-end control element and the bank of disk drives (e.g., Figure 2; Column 2, lines 50-63). Although Walton et al do not specify a SAN interface coupled to said disk drive for coupling the front-end control element to the back-end control element, Walton et al show the inclusion of a bus interface (e.g., Figure 4), which is coupled to the disk drive bank and to Bus D, providing for the exchange of information between the front-end control element and the back-end control element (e.g., Figure 2). It would have been obvious at the time the invention was made to a person having ordinary skill in the art with the teachings of Walton et al and Brown et al to incorporate a back-end control element comprising a disk drive

interface coupled to the back-end control element and the disk drive and a SAN interface coupled to the disk drive interface and the front-end control element because it would result in a communication link among the front-control element, the back-control element, and ultimately the plurality of disk drives.

With respect to Claims 15-18 and Claims 20-23, Walton et al and Brown et al teach Claim 14. However, Walton et al do not teach the required element within the SAN interface. Brown et al, however, teach the use of an interconnect element comprising preferably of a Fibre Channel switch coupled to a Fibre Channel communication medium (e.g., Figure 2; Column 6, lines 20-66). Furthermore, Brown et al suggest that a Fibre Channel communication medium is preferable, but also suggest the use of PCI buses and imply the use of other communication mediums (e.g., Column 6, lines 31– 43). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to further include one of the following within the mentioned SAN interface of the control element in Claim 14 or Claim 19: a PCI bus interface, a Fibre Channel communication media interface, an Infiniband compliant communication medium, or a local area network communication medium. Inclusion of any of the above mentioned interfaces or mediums would aid in the exchange of information due to the selected interconnect medium used to link the front-end control element to the back-end control element.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Belsan, United States Patent No. 5394532

b) Brown et al, United States Patent No. 6148414

c) Iwatani, United States Patent No. 6023780

d) Walton et al, United States Patent No. 6389494 B1

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kathy Takeguchi whose telephone number is (703) 305-8115. The examiner can normally be reached on Monday - Friday, 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

PB
September 12, 2002

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100